



10/696,598.

PTO/SB/21 (09-04) (AW 10/2004)

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TRANSMITTAL FORM <i>(to be used for all correspondence after initial filing)</i>	U.S. Patent No.	6,983,538 B2
	Issued	January 10, 2006
	First Named Inventor	Masafumi Inoue et al.
	Art Unit	
	Examiner Name	
Total Number of Pages in This Submission	Attorney Docket No.	MAT-8184US1

ENCLOSURES (Check all that apply)		
<input type="checkbox"/> Fee Transmittal Form <input type="checkbox"/> Fee Attached <input type="checkbox"/> Amendment/Reply <input type="checkbox"/> After Final <input type="checkbox"/> Affidavits/Declaration(s) <input type="checkbox"/> Extension of Time Request <input type="checkbox"/> Express Abandonment Request <input type="checkbox"/> Information Disclosure Statement <input type="checkbox"/> Certified Copy of Priority Document(s) <input type="checkbox"/> Response to Missing Parts/ Incomplete Application <input type="checkbox"/> Response to Missing Parts under 37 CFR 1.52 or 1.53	<input type="checkbox"/> Drawing(s) <input type="checkbox"/> Licensing-related Papers <input type="checkbox"/> Petition <input type="checkbox"/> Petition to Convert to a Provisional Application <input type="checkbox"/> Power of Attorney, Revocation, Change of Correspondence Address <input type="checkbox"/> Terminal Disclaimer <input type="checkbox"/> Request for Refund <input type="checkbox"/> CD, Number of CD(s) _____ <input type="checkbox"/> Landscape Table on CD	<input type="checkbox"/> After Allowance Communication to TC <input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences <input type="checkbox"/> Appeal Communication to TC (Appeal Notice, Brief, Reply Brief) <input type="checkbox"/> Proprietary Information <input type="checkbox"/> Status Letter <input checked="" type="checkbox"/> Other Enclosure(s) (please identify below): Request for Certificate of Correction PTO Form 1050 Return Postcard
Remarks:		

Certificate

MAR 31 2006

of Correction

SIGNATURE OF APPLICANT, ATTORNEY OR AGENT			
Firm Name	RatnerPrestia		
Signature			
Printed Name	Lawrence E. Ashery		
Date	March 27, 2006	Registration No.	34,515

CERTIFICATE OF TRANSMISSION / MAILING			
I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.			
Signature			
Typed or Printed Name	Deborah Spratt	Date	March 27, 2006

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APR 03 2006

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Patent Number: 6,983,538 B2
January 10, 2006
Name of Patentee: Masafumi Inoue et al.
Title of Invention: METHOD OF MOUNTING COMPONENT ON A CIRCUIT BOARD

REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT
FOR PTO MISTAKE (37 C.F.R. § 1.322(a))

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attention: Decision and Certificate of Correction
Branch of the Patent Issue Division

1. Attached in duplicate is Form PTO-1050 with at least one copy being suitable for printing.
2. Correction of the Official Letters Patent is respectfully requested in view of the following text which appears correctly in the application file:

Column 6, lines 21-49, claims 4-7, delete

"4. A method of mounting components on a board, said method comprising the steps of:

- a) receiving mounting locations of where said components are intended to be mounted on said board,
- b) determining where solder for said components is situated on said board,
- c) determining where said components are to be mounted on said board based on steps a) and b); and
- d) mounting said components on said board based on step c).

5. A method of mounting components according to claim 4, wherein step c) includes the step of modifying said mounting locations based on step b), wherein said components are mounted in step d) based on said modified mounting locations.

6. Apparatus for mounting components on a board, comprising:
 - a memory in which is situated location values which correspond to where components are intended to be mounted on said board;
 - a locator for identifying solder locations which correspond to respective locations of solder on said board;
 - a mounter for mounting said components based on said location values and said solder locations.

APR 03 2006

7. Apparatus for mounting components according to claim 6, further comprising a calculation unit which modifies said location values based on said solder values, wherein said mounter mounts said components based on said modified location values."

as written in the Supplemental Preliminary Amendment dated October 29, 2003, page 3, line 33, claims 9-12. Amendment claims 9-12 are Patent claims 4-7.

3. Please send the Certificate to:

Name: Lawrence E. Ashery
P.O. Box 980
Valley Forge, PA 19482
(610) 407-0700

Name of Assignee: Matsushita Electric Industrial Co., Ltd.

Assignment Recorded on: January 4, 2002

Reel: 012433

Frame: 0728

Respectfully submitted,

Lawrence E. Ashery, Reg. 34,515
Attorney for Applicants

LEA/ds

Enclosure: Form PTO-1050 (in duplicate)

Dated: March 27, 2006

P.O. Box 980
Valley Forge, PA 19482
(610) 407-0700

The Commissioner for Patents is hereby authorized to charge payment to Deposit Account No. **18-0350** of any fees associated with this communication.

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March 27, 2006

Deborah Spratt

Deborah Spratt

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**UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION**

PATENT NO: 6,983,538 B2
APPLICATION NO.: 10/696,598
DATED: JANUARY 10, 2006
INVENTOR(S): MASAFUMI INOUE ET AL.

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 6

Lines 21-49, claims 4-7, delete

"4. A method of mounting components on a board, said method comprising the steps of:
a) receiving mounting locations of where said components are intended to be mounted on said board,
b) determining where solder for said components is situated on said board,
c) determining where said components are to be mounted on said board based on steps a) and b); and
d) mounting said components on said board based on step c).

5. A method of mounting components according to claim 4, wherein step c) includes the step of modifying said mounting locations based on step b), wherein said components are mounted in step d) based on said modified mounting locations.

6. Apparatus for mounting components on a board, comprising:
a memory in which is situated location values which correspond to where components are intended to be mounted on said board;
a locator for identifying solder locations which correspond to respective locations of solder on said board;
a mounter for mounting said components based on said location values and said solder locations.

7. Apparatus for mounting components according to claim 6, further comprising a calculation unit which modifies said location values based on said solder values, wherein said mounter mounts said components based on said modified location values."

Mailing Address of Sender:

RatnerPrestia
P.O. Box 980
Valley Forge, PA 19482
(610) 407-0700

This collection of information is required by 37 CFR 1.322, 1.323 and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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**UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION**

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Lines 21-49, claims 4-7, delete

"4. A method of mounting components on a board, said method comprising the steps of:
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c) determining where said components are to be mounted on said board based on steps a) and b); and
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